

**XP-002291220**

**AN - 1981-N0462D [51]**

**CPY - MOTD**

**DC - U14**

**FS - EPI**

**IC - G11C7/00**

**IN - KOSOV L I; KOSOV V I; SAVELEV A I**

**MC - U14-A07**

**PA - (MOTD ) MOSC TEXTILE INST**

**PN - SU809350 B 19810228 DW198151 004pp**

**PR - SU19792771909 19790531**

**XIC - G11C-007/00**

**AB - SU-809350 Multiple signal strobing and different readout timing are deployed in the computer memory to reduce random error. The circuit uses logic gates, triggers, strobe pulse formers, discriminators and additional readout amplifiers.**

- The storage readout signals are applied simultaneously to the main and additional read-out amplifiers triggering a delay controlling strobe pulse formers for the amplifiers. The same signal is read twice. Discrimination level formers operate discriminators, further differentiating the readout.

- On non-coincidence of the signal former contents, the additional controls initiate digit-by-digit data comparison to detect the errors. Multiple sensing of the same storage signal avoids accidental false readout of the stored data. Bul.8/28.2.81 (4pp)

**IW - MEMORY DIGITAL COMPUTER MULTIPLE SIGNAL STROBE READ-OUT TIME REDUCE ERROR**

**IKW - MEMORY DIGITAL COMPUTER MULTIPLE SIGNAL STROBE READ-OUT TIME REDUCE ERROR**

**INW - KOSOV L I; KOSOV V I; SAVELEV A I**

**NC - 001**

**OPD - 1979-05-31**

**ORD - 1981-02-28**

**PAW - (MOTD ) MOSC TEXTILE INST**

**TI - Memory for digital computers - uses multiple signal strobing and read=out at different times, reducing errors**